MORION

RFS-M102

User's guide

Rev. 1.2A

Contents

Document Revision history

THIS DOCUMENT REVISION	DESCRIPTION	FW REVISION	HW REVISION	DATE
0.1A	Initial issue	FPGA_1.2 200420	1	24.04.2020
0.2A	Communication protocol joined	FPGA_1.2 060520	1	12.05.2020
0.3A	Common mistakes fixed	FPGA_1.2 060520	1	21.05.2020
0.4A	Language review	FPGA_1.2 060520	1	25.05.2020
1.0A	First issue for distribution	FPGA_1.2 250520	1	15.06.2020
1.1A	LVCMOS levels specified	FPGA_1.2 250520	1	08.07.2020
1.2A	**LOCK levels detailed spec added**	**FPGA_1.2 250520**	**1**	**10.08.2020**

1. Introduction

1.1. Purpose

This manual is intended for engineers who design and operate compact Rb oscillator based equipment. The main purpose of this document is to provide the engineers the best practice of designing and operating Rb oscillators to get great performance.

1.2. Safety

Caution! The temperature of the unit case during operation may rise up to 90°C. In order to avoid skin damage, exercise caution.

RFS-M102 is an ESD sensitive device.

2. RFS-M102 Rubidium Frequency Standard

2.1. Overview

2.1.1. T1 Case drawing and pin designation

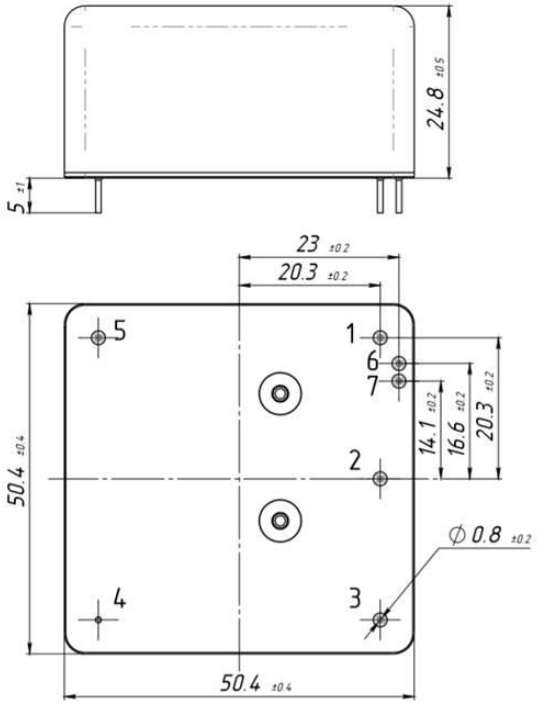

Figure 1. T1 case drawing

Table 1. T1 case Pin designation

PIN #	FUNCTION
1	Multipurpose pin (**1PPS input by default**)
2	Multipurpose pin(**1PPS output by default**)
3	RF output
4	GROUND (SIGNAL+CASE)
5	Power supply input
6	DATA TX (UART)
7	DATA RX (UART)

2.1.2. RFS-M102 default specification

Table 2. Main parameters

#	PARAMETER	DEFAULT SPECIFICATION	NOTES
1	Frequency	10 MHz	Other frequencies available upon request
2	Output signal	SIN	
3	Output power	>7dBm	50 Ohm load
4	Harmonics	<-30 dBc	
5	Spurious	<-60 dBc	
6	Digital frequency tuning range	±1E-7	
7	Voltage supply	12V	11.8 – 12.2V at Pin #5
8	Power consumption	20W max (18W typical) during warm-up 6W steady state	Steady state power value is rated for maximum operating temperature
9	Warm-up time @ 25ºC	<5min to LOCK <7.5min to ±1E-9 <15min to ±5E-10	25°C is initial case temperature, heat sinking is less than 5W
10	Allan deviation	<5E-11@1s, <2E-11@10s, <8E-12@100s	at constant temperature (<±2°C), after 2h of continuous operation
11	Phase noise	-80dBc/Hz@10Hz -115dBc/Hz@100Hz -130dBc/Hz@1000Hz	after 2h of continuous operation
12	Long-term stability	±2E-11/day*, ±1E-9/year*	*Average value of 7 days continuous operation at constant temperature(<±2°C) after 24 h of continuous operation
13	Frequency vs. temperature stability	±3E-10	
14	Retrace	<±5E-11	24h ON -> 6h OFF ->2h ON
15	Input voltage sensitivity	<±2E-11	11.8 to 12.2VDC
16	Weight	<150g	

2.1.3. List of available options

Required options should be chosen when placing an order.

Table 3. Option list and description

#	DESIGNATOR	SPEC	COMMENT
1	Operating temperature range *RFS-M102-**XX**XXX-XXX-XX-10MHz-X*		
	HU (default)	-10* to 75 baseplate temperature	*Unit may start at -10°C (-40°C) baseplate and continue operation at -10°C (-40°C) ambient temperature with total heat sinking less than 5W. ***Unit overheating may cause severe damage of the device. See recommendations on heat sinking in Section 0.***
	HV	-10* to 80 baseplate temperature	
	EU	-40* to 75 baseplate temperature	
	EV	-40* to 80 baseplate temperature	
2	Frequency vs. temperature stability *RFS-M102-XX**XX**X-XXX-XX-10MHz-X*		
	01	±1E-10	F vs T stability is calculated as $df_t = \pm (f_{max} - f_{min}) / 2f_{nom}$ f_{nom} *is nominal output frequency (10MHz)*
	02	±2E-10	
	03 (default)	±3E-10	
3	Long-term-stability options *RFS-M102-XXXX**X**-XXX-XX-10MHz-X*		
	A (default)	±2E-11/day*, ±1E-9/year**	*Average value of 7 days continuous operation at constant temperature(<±2°C) after 24 h of continuous operation **After 30 days of continuous operation
	B	±4E-12/day*, ±5E-10/year**	
4	Output signal form *RFS-M102-XXXXX-**XXX (or XXXXX)**-XX-10MHz-X*		
	SIN (default)	Sinusoidal	
	LVCMOS	Square-wave	3.3V LVCMOS
5	Package type *RFS-M102-XXXXX-XXX-**XX**-10MHz-X*		
	T1	7 pin case	See Figure 1 and Table 1
6	Additional options *RFS-M102-XXXXX-XXX-XX-10MHz-**X***		
	-(default)	Pin #1 and Pin #2 are Multipurpose pins	Pin#1 The functionality of pin #1 is assumed to become user programmable in future**:** 1 – 1 PPS input (**default**) 2 – Factory purpose (left blank for future improvements) Pin#2 The functionality of pin #2 is user programmable with Command #88. Following states are available: 1 – 1 PPS output (**default**) 2 – 1 PPS output inverted 3 – Constant HIGH level (3.3V) 4 – Constant LOW level (0V) 5 – Lock bit, heating status and others selected by Command #19 (See section 2.2.3) 6 - I**nverted** Lock bit, heating status and others selected by Command #19 (See section 2.2.3) ***Note 1: Configuration is stored in FLASH, which has 10 000 cycles lifetime.***
	A	Analog tuning option ±1.5E-9. Pin #2 stays Multipurpose	***Note 1:*** *This option is not compatible with the default auxiliary option. This option cannot be disabled once installed.* ***Note 2:*** *Unit is factory calibrated at 2.6±0.2V. Unit has internal weak pull up to 2.6V.*

2.1.4. Absolute Minimum and Maximum values

Table 4. Absolute Minimum and Maximum electrical values

PIN #	TYPE	SPEC
Pin#1	Input	0 – 5 V
Pin#2 minimum load / compatibility	Output	10 kOhm, 3.3V LVCMOS compatible
Pin#3 load	Output	50 Ohm±10%
Pin#4	GROUND (SIGNAL+CASE)	GROUND (SIGNAL+CASE), 0V
Pin#5 voltage	Power	11.8 – 12.2 V
Pin#6 minimum load	Output	10 kOhm, LVCMOS compatible
Pin#7 voltage	Input	0-3.3 V

2.2. Principle of operation

2.2.1. Rb oscillator design description

RFS-M102 is a compact passive lamp pumped Rb frequency standard. After power on it performs a sequence of actions required to let internal TCXO lock to the highly stable atomic transition in Rb^{87} atomic structure using double microwave resonance technique. See section 0 for details.

This is a so called “traditional” scheme of the Rb vapor atomic clock, which has an exceptional reliability proved by the decades of operation in commercial and space applications.

Rb lamp emits waves, which are absorbed by the Rb cell. The intensity of the absorption is regulated by a microwave field, which is applied to the cell. If the field’s frequency equals atomic resonance frequency cell exhibits maximum absorption. In this case, PLL locks microwave field to an atomic transition. Actually, it is not the microwave signal itself that is locked, but a lower frequency VCTCXO oscillator that is multiplied to a microwave level. This VCTCXO is also used for Rb oscillator output signal generation.

In order to calibrate unit’s frequency or manually add a small offset to the output frequency, an additional DDS frequency is mixed with a TCXO signal. So, if DDS frequency is changed, TCXO frequency also changes, as soon as offset frequency should remain constant to stay in atomic resonance.

Several factors could vary atomic transition frequency. Here are most significant of them:

- Lamp bulb temperature and light intensity

- Rb cell temperature

- Ambient magnetic field variation

Lamp and cell temperatures are closely coupled with Rb vapour pressure inside them. In order to keep Lamp and Rb cell temperatures stable, both are placed in heat ovens at constant temperatures. The ovens are tuned to different temperatures and require different time for temperature stabilization depending on mounting design and environmental conditions.

An appropriate atomic sublevels splitting is required for resonance detection. An internal magnetic field cause Zeeman effect and splits the sublevels. However, the amplitude of the field should stay constant to keep resonance frequency stable. This effect laid into principle of operation of the analog tuning (an auxiliary option): slow changes of the magnetic field amplitude cause changes in the output frequency of the unit.. External magnetic field variation is mostly suppressed by double magnetic shielding of the unit. Instability vs external magnetic field is not specified for the unit.

Output frequency is locked to atomic resonance when atomic signal exceeds a preset value. Normally it happens prior to ovens temperature stabilization. So output frequency variation may continue until lamp and cell temperatures are stabilizing. Refer to bits 20 and 21 in status register to check when stabilization is finished.

2.2.2. Start-up Sequence

RFS-M102 has the following internal initialization:

Table 5. Start-up sequence

STEP	REGIME	CURRENT, TYPICAL	TYPICAL TIME FROM POWER UP
1	Getting into optimal Lamp ignition temperature range	~1.5A (or 0.3A)	less than 2 minutes
2	Lamp ignition	~0.4A	less than 3 minutes
3	Continue heating the ovens and Searching for resonance	~1.5A	less than 4 minutes
4	Atomic resonance quality is good, locking	<1A	less than 4 minutes

It is recommended to wait for at least 10 minutes before next power up.

2.2.3. Status register

Status register contains basic telemetry information of the unit, such as PID states, heating elements states, 1PPS lock etc.

Table 6. Status register description

BIT #	BIT NAME	DESCRIPTION	NORMAL STATE
0	Undefined		
1	Undefined		
2	Undefined		
3	Undefined		
4	Lamp PID enabled	1 - Lamp temperature regulation is enabled 0 - Lamp temperature regulation is disabled	Normally Enabled. However, during warm-up period it could be disabled automatically for a cool down period.
5	Rb cell PID enabled	1 - Rb cell temperature regulation is enabled 0 - Rb cell temperature regulation is disabled	Normally Enabled. However, during warm-up period it could be disabled automatically for a cool down period.
6	Undefined		
7	Factory purpose bit		
8	Undefined		
9	Undefined		
10	Undefined		
11	Undefined		
12	Undefined		
13	Undefined		
14	Undefined		
15	Undefined		
16	Unit locked bit	1 – Output frequency is locked to a high stable Rb^{87} atomic transition 0 – Unit is searching for a high stable Rb^{87} atomic transition	Normally logic 1 at operation.
17	Factory purpose bit		
18	Factory purpose bit		
19	Lamp cool down flag	0 – Lamp is not cooling down 1 – Lamp is cooling down	0
20	Hot lamp flag	0 – Lamp temperature variations are too high or current temperature is out of ±0.5°C region 1 – Lamp temperature variations are low enough and current temperature is within ±0.5°C region	1
21	Hot cell flag	0 – Lamp temperature variations are too high or current temperature is out of ±0.5°C region 1 – Lamp temperature variations are low enough and current temperature is within ±0.5°C region	1
22	Factory purpose bit		
23	Locked to external 1 PPS flag	0 – Unit is not locked to external 1 PPS 1 – Unit is locked to external 1 PPS Unit is considered as LOCKED to 1 PPS if there is less than ±50 ns time difference for at least 1 hour	1 if tracking is enabled, otherwise, 0
24	Multi-purpose output pin enabled	Multipurpose output bit is available by default	1- default value
25	1 PPS input tracking enabled	0 – Tracking is disabled (Free run mode) 1 - Tracking is enabled (1 PPS sync mode)	
26	Factory purpose bit		
27	Undefined		
28	Undefined		
29	Undefined		
30	Undefined		
31	Undefined		

Note: Bit #0 is LSB

Status register is available via UART. See List of commands

2.3. Interface characteristics

2.3.1. Frequency adjustment, synchronization and calibration

2.3.1.1. Analog tuning

Note! This function is not installed by default. Please, refer to ordering guide.

The principle of analog frequency tuning is based on weak non-linear magnetic dependence of the atomic frequency. As soon as internal magnetic field is required for unit operation, small variation of its magnitude will cause small variation in the output frequency.

If Analog option is applied, nominal frequency of the unit will be reached in a 2.6±0.2V range of the input voltage. If pin is left floating, self-biasing will keep the input voltage at 2.6±0.2V.

2.3.1.2. Digital tuning

Digital tuning is installed as the default method of frequency tuning as it is robust, reliable and noiseless. In addition, it allows saving frequency offset value to non-volatile memory. See section 2.4 for details.

2.3.1.3. 1 PPS input

1 PPS signal from a stable source may be applied to Pin#1 in order to achieve excellent long-term behavior. Synchronization time depends on the internal PID regulator settings, initial frequency offset and 1PPS signal stability. Also, unit can be calibrated using 1PPS signal using Command #18. See section 2.5.1 for details.

2.3.1.4. 1 PPS output

Unit can be a source of synchronization pulses for different devices. Depending on customer design requirements, 1PPS output mode could be either direct (Pulse level HIGH) or inverted (Pulse level LOW). See section 2.5.2 for details.

2.3.1.5. LOCK indicator and other status bits

Refer to section 2.2.3 for full description of available status flags. Any bit from the register could be forwarded to Pin #2. Use Command #19 to select the required bit and command #88 to switch to a certain Pin #2 output mode.

Table 7. Pin #2 signal if LOCK bit is selected as output pin bit

	SIGNAL AT PIN#2	UNIT IS LOCKED	
		NO (Bit #16 is 0)	YES (Bit #16 is 1)
PIN #2 MODE	LOCK OUTPUT (MODE 5)	Constant Logic HIGH	Constant Logic LOW
	LOCK OUTPUT INVERTED (MODE 6)	Constant Logic LOW	Constant Logic HIGH

2.4. Interfacing the World

2.4.1. Serial communication protocol

Caution! Internal FLASH memory lifetime is 10 000 cycles. Using any of the “SAVE to NON VOLATILE memory commands” over 10 000 times will make unit not operable. However, 10 000 cycles is more than adequate for unit operation over 10 years.

See Appendix A. FPGA Interface Protocol (Rev.07) for details.

2.5. Design guide

2.5.1. 1PPS disciplining settings

1 PPS input is available by default (if Analog tuning option is not selected). See ordering guide for details. Also, refer to Serial Communication Protocol for details on how to switch on 1PPS input if disabled. Typically, RFS-M102 has less than 1us/day timing error. However, for some applications a better performance is required. One pulse per second signal can be used for disciplining the unit to a more accurate reference. GPS signal, passive or active hydrogen standard, Cesium standard, etc. could be such a reference. Depending on the short-term and middle-term stability of the reference, different synchronization time will be required. For example, GPS 1 PPS specification is ~±50 ns, which means that several hours of averaging will be required to get the stability of the order of the Rb oscillator *(which at such averaging time will show appox. 5E-13 or less at constant temperature).* In this case, time constant should be high enough *(8 thousands and more. See table below).* Another situation is, for instance, using a hydrogen standard, which has excellent short-term and long term stability so that we can rely on every 1PPS pulse we detect and use it to slightly adjust our unit's frequency.

An example:

Let's consider that default 1PPS input settings are applied.

If the input reference shifts by +100ns, the proportional term (default value 200) will adjust the offset tuning word by 200bits/2.16ns * 100ns = -9259 bits. Each bit of the tuning word corresponds to 1.57 10^{-14} of the operating frequency, and so the RFS-M102 frequency will be shifted by about 9259x1.57 x 10^{-14} by the next second (or by the chosen averaging time). The integral term (default value 2) will begin ramping by -2bits/s(or by-2 bits in a selected averaging time)) 7200 bits/hour until phase shift is more than zero. If it stays zero integral term will not work. The phase shift between the 1pps input and 1pps output will be gradually eliminated.

Phase jumps of 100ns are quite common on 1pps outputs from GPS receivers, which are a frequent 1pps reference. The corresponding frequency jumps of N x 10^{-11} may be excessive in some applications, and so an averaging pre-filter is used to smooth the time-tag values before they are used by the PLL algorithm. See Command #82. Increasing correction interval may help in this case.

Command #82 is used to set the current PPS change rate from the list:

Table 8.1PPS input averaging

STATE	AVERAGING TIME, S
0	1(**default**)
1	16
2	128
3	512
4	2048
5	8192
6	32768

1PPS tracking algorithm has the following sequence

Table 9.1PPS tracking algorithm

STEP	DESCRIPTION
1	After unit is locked and heated (corresponding bits 20 and 21 are high) start searching for 2 input pulses which get into ±50ns interval. For example, if unit and reference frequencies differ by more than 5E-8 they could not be synchronized. In this case, use digital tuning first.
2	Synchronize internal 1pps to the next received pulse
3	Start calculating phase difference (or so-called “gate”) between incoming 1pps and internal 1pps signal. If next 16 gates are less than ~±500ns, PID regulator starts adjusting frequency of the Rb oscillator. If not (in case when frequency difference is too much), reset and go to item 1
	Note. 500ns in 16 seconds means that frequency difference is at least ±3.1E-8.

1PPS input lock bit (bit #23 in status register) gets high if phase difference between incoming 1PPS signal and internal 1PPS signal is less than ±50 ns within an hour. If in a certain moment phase difference exceeds this limit hour counter will be reset.

1PPS input pulse should have at least 1 us length. Recommended logic values are U < 0.5V for Logic 0 and 2.8V < U < 5V for Logic 1.

2.5.2. 1PPS output

Depending on the selected mode of the Multipurpose PIN #2 unit can provide 1 PPS signal for external device synchronization Mode 1 (non inverted 1PPS output) has the following signal profile:

> Logic HIGH level for ~10us and logic LOW level for ~999 990 us. This is a default mode for unit operation. 1PPS output **inverted** mode (mode 2) has the following signal profile: logic LOW level for ~10us and logic HIGH level for ~999 990 us.

Table 10. Pin #2 signal for different modes of operation

	SIGNAL AT PIN#2	UNIT IS LOCKED AND HEATED UP	
		NO	YES
PIN #2 MODE	1PPS OUTPUT (MODE 1)	Constant Logic HIGH	1PPS signal
	1PPS OUTPUT INVERTED (MODE 2)	Constant Logic LOW	1PPS signal inverted (Pulse level LOW)

Pin #2 is 3.3V LVCMOS compatible. Recommended load value is indicated in Table 1.

1PPS output is the most universal function of the unit as it provides both Lock status and 1 PPS output signal consequently.

2.5.3. Thermal considerations

In order to keep Lamp and Rb cell temperatures stable, both are placed in heat ovens at constant temperatures. However, those optimal temperatures have about 40°C difference.

Closed area inside a miniature oscillator doesn't allow to make the ovens completely independent, so a part of the extra heat is drained to the unit case to prevent overheating of the colder oven. This is quite common solution for such kind of devices.

During operation Rb oscillator consumes about 4-6W of power, depending mostly on environmental conditions and mounting. Most of the energy is dissipated via heat flow throw the unit's case to the surrounding environment. The environment should be able to handle and dissipate this heat flow so that case temperature will never exceed maximum allowable value.

Having an infinite number of possible designs of the equipment, with or without heatsinks, still air or with a sufficient air flow, closed area or caseless units etc. the only adequate criteria for setting operation temperature range of the unit is referring to baseplate temperature, which should not exceed the threshold, which equals maximum operating temperature (defined by selected temperature range option).

The unit allows getting telemetry information on its status and it is strongly recommended that the engineer use this information to eliminate overheating of the unit during product development stage.

It is a good practice to use thermal conductive material between unit case and PCB. Sil-Pad 900 or similar.

Please, consult factory, for heat sink recommendations and suggested thermal pad materials.

2.5.4. Electrical interface

2.5.4.1. Input power

The input power is 12±0.2V at pin. Please, note, that the wires should be qualified for transferring at least 1.5A. Keep in mind possible voltage drop during warm up period as soon as current reaches its maximum during this period. It voltage drops below ~11.8V, unit may restart or work unstable.

2.5.4.2. Communication interface settings

UART RX and TX signals are used to communicate with the unit for the purpose of controlling and monitoring. RX and TX are 3.3V LVCMOS compatible. The following settings should be used for communication

- Baud rate: 9600
- Characters: 8 bits
- Parity: none
- 1 stop bit

Also, please, keep in mind wire length, which may affect signal properties and cause failure of the serial interface (recommended wire length is less than 0.5m).

2.5.5. Troubleshooting

If the unit fails to lock or doesn't responding to communication commands, verify the following:

- The voltage at Vcc pin (pin 5) is not out of recommended values
- Power supply current limit is more than current required for unit operation
- The case temperature is lower than maximum and higher than minimum
- Serial communication settings and levels are not out of recommended values

2.5.6. Firmware upgrade

RFS-M102 supports firmware upgrade via RS232. Contact factory for details.

2.5.7. ERRATA

ISSUE#	DESCRIPTION	TYPE OF ERROR	FOUND IN FW REVISION #	FIXED IN FW REVISION #
1	Wrong temperature sensor values at low temperatures at start-up	Not affect operation	1.1	1.2

Appendix A. FPGA Interface Protocol (Rev.07)

Revision history

REV. #	DESCRIPTION	DATE	FW REVISION
00	Initial release	19/07/2019	-
01	Factory commands removed	29/10/2019	-
02	Common mistakes in examples fixed	10/12/2019	-
03	Status register command added	13/12/2019	V1.0_251219
04	Command #13 purpose changed, Command #14 added, Command #04 description updated	31/01/2020	V1.0_251219
05	Commands #13 and #14 description corrected, document header updated (interval requirement, FLASH lifetime)	14/02/2020	V1.1_170220
06	Commands #18, #81-88 added, boundary values verification added for 1PPS commands	20/04/2020	V1.2_200420
07	Command #88 functionality updated, Command #19 added, Command #81 name changed	06/05/2020	V1.2_060520

Purpose

This section describes serial interface protocol for universal asynchronous port (UART) of the RFS-M102 rubidium frequency standard.

Start of communication

The communication is self-activated in 5 seconds after power-up. The unit works in slave mode.

Each command starts with unique string “?DEV:” followed by two bytes of command ID, then character ‘:’ or ‘?’ in write or read case respectively. If request command is performed DATA bytes will be returned by the unit. Carriage-return/line-feed combination (<CR/LF> 0x0D/0x0A) completes each transition.

All data in a message, except commands 01 and 02, must be limited to “0123456789ABCDEF” symbols (hex

number format). An interval of at least 500ms between two consequent commands is required for proper and

expectable operation.

FLASH lifetime is 10 000 write cycles.

Communications Setup

Baud: 9600bits/s

Data bits: 8

Stop bits: One

Parity: None

WARNING: the unit supports 3.3V logic levels

List of commands

COMMAND ID	COMMAND NAME	TYPE	INPUT	RESPONSE	REMARKS	EXAMPLE
01	Unit Number	Request	?DEV:01?<CR/LF>	?DEV:01:***<CR/LF>	This command is used to read the Unit Number from non-volatile memory.	?DEV:01:MT0015<CR/LF>
02	Firmware Version	Request	?DEV:02?<CR/LF>	?DEV:02:***<CR/LF>	This command is used to read the Factory Firmware Version from non-volatile memory. Where *** - is 24 ASCII symbols maximum	?DEV:02:FPGA_V1.0_061219<CR/LF>
03	Status Register	Request	?DEV:03?<CR/LF>	?DEV:03:XXXXXXXX<CR/LF>	Status register: 0 – 3:reserved; 4:Lamp PID Enable; 5:Cell PID Enable; 6: reserved; 7: factory command; 8-15: reserved; 16:Unit Locked; 17:factory command; 18:factory command; 19:factory command; 20:factory command; 21:factory command; 22:factory command; 23:Ext. 1PPS Lock; 24:1PPS out enabled; 25:1PPS in enabled; 26:factory command; 27-31: reserved	?DEV:03:003580B0<CR/LF>
04	Save Flash	Set	?DEV:04?<CR/LF>	?DEV:OK<CR/LF>	Save data from RAM to non-volatile memory. Specified data will be ignored. See other commands description for details	?DEV:04?<CR/LF>

COMMAND ID	COMMAND NAME	TYPE	INPUT	RESPONSE	REMARKS	EXAMPLE
13	Frequency Offset (Save to FLASH, READ from FLASH)	Set	?DEV:13:XXXXXXXX<CR/LF>	?DEV:OK<CR/LF>	This command is used to set the current frequency offset to FLASH **and** to RAM (i.e. applied immediately). XXXXXXXX is a 8 Byte offset word in HEX. The value will be loaded from FLASH to RAM at STARTUP. If command is applied, the sent value will replace "current frequency offset", stored in RAM	One bit corresponds to 1.597e-14 parts of Nominal Output Frequency. For 10MHz output: To make a +1 Hz offset: X = dec2hex(int (1 Hz/10000000Hz/1.597e-14)) = 5F8BED h The command to enter is **?DEV:13:005F8BED<CR/LF>** To make a -0.05 Hz offset: X = dec2hex(int (-0,05 Hz/10000000Hz/1.597e-14)) = FFFB3901 h The command to enter is **?DEV:13:FFFB3901<CR/LF>** **VALUES HIGHER THAN ±1HZ (005F8BED / FFA07413) WILL BE IGNORED**
		Request	?DEV:13? <CR/LF>	?DEV:13:XXXXXXXX<CR/LF>	This command reads SAVED TO FLASH frequency offset. XXXXXXXX is a 8 Byte offset word in HEX	For a -0.05Hz offset unit will return: ?DEV:13:FFFB3901<CR/LF>
14	Frequency Offset (Save to RAM, READ from RAM)	Set	?DEV:14:XXXXXXXX<CR/LF>	?DEV:OK<CR/LF>	This command is used to set the current frequency offset to RAM. XXXXXXXX is a 8 Byte offset word in HEX. ***Note 1:*** *Command #04 will ignore an offset made by this command and will not save the value to FLASH*	One bit corresponds to 1.597e-14 parts of Nominal Output Frequency. For 10MHz output: To make a +1 Hz offset: X = dec2hex(int (1 Hz/10000000/1.597e-14)) = 5F8BED h The command to enter is **?DEV:13:005F8BEC<CR/LF>** To make a -0.05 Hz offset: X = dec2hex(int (-0,05 Hz/10000000/1.597e-14)) = FFFB3901 h The command to enter is **?DEV:13:FFFB3901<CR/LF>** **VALUES HIGHER THAN ±1HZ (005F8BED / FFA07413) WILL BE IGNORED**
		Request	?DEV:14? <CR/LF>	?DEV:14:XXXXXXXX<CR/LF>	This command reads the current frequency offset from RAM. XXXXXXXX is a 8 Byte offset word in HEX	For a -0.05Hz offset unit will return: ?DEV:14:FFFB3901<CR/LF>

COMMAND ID	COMMAND NAME	TYPE	INPUT	RESPONSE	REMARKS	EXAMPLE
18	1PPS Offset word	Set	?DEV:18?<CR/LF>	?DEV:OK<CR/LF>	This command is used to calibrate a unit to a 1PPS input signal. Current frequency difference will be saved to FLASH.	
19	Main status bit selection	Set	?DEV:19: 000000XX <CR/LF>	?DEV:OK<CR/LF>	This command sets one of the status bits as main, which means the bit could be multiplexed to multifunctional pin using Command #88. Possible data values are : 00-1F which correspond to number of bit in status register	
		Request	?DEV:19? <CR/LF>	?DEV:19:000000XX<CR/LF>	This command is used to read the current FPGA output mode.	
81	Multifunctional input pin mode	Set	?DEV:81: 0000000X <CR/LF>	?DEV:OK<CR/LF>	This command is used to enable/disable External 1PPS tracking. Where X is 1 (enable) or 0 (disable).	
		Request	?DEV:81?<CR/LF>	?DEV:81:0000000X<CR/LF>	This command is used to read the current External 1PPS state. Where first 7 bytes are zero, and the last byte is current state (1 – enabled, 0 – disabled).	

COMMAND ID	COMMAND NAME	TYPE	INPUT	RESPONSE	REMARKS	EXAMPLE
82	1 PPS averaging time	Set	?DEV:82:0000000X <CR/LF>	?DEV:OK<CR/LF>	This command is used to set the current averaging of the 1 PPS signal. The more noisy the signal is the higher change rate should be applied: 0: Change rate = 1 sec; 1: Change rate = 16 sec; 2: Change rate = 128 sec; 3: Change rate = 512 sec; 4: Change rate = 2048 sec; 5: Change rate = 8192 sec; 6: Change rate = 32768 sec.	
		Request	?DEV:82?<CR/LF>	?DEV:82:0000000X<CR/LF>	This command is used to read the current PPS change rate.	
83	1PPS PID Integral Coeff	Set	?DEV:83:0000XXXX <CR/LF>	?DEV:OK<CR/LF>	This command is used to set the current 1PPS PID integral coeff (Ki). XXXX – 4 bytes with signed data. Most significant bit is the sign.	?DEV:83:1FFF – positive number, ?DEV:83:AFFF – negative number
		Request	?DEV:83?<CR/LF>	?DEV:83:0000XXXX<CR/LF>	This command is used to read the current 1PPS PID integral coeff (Ki). Where first 4 byte are zero, and 4 last byte is a message.	
84	1PPS PID Proportional Coeff	Set	?DEV:84:0000XXXX <CR/LF>	?DEV:OK<CR/LF>	This command is used to set the current 1PPS PID proportional coeff (Kp). XXXX – 4 bytes with signed data. Most significant bit is the sign.	?DEV:84:1FFF – positive number, ?DEV:84:8FFF – negative number
		Request	?DEV:84?<CR/LF>	?DEV:84:0000XXXX<CR/LF>	This command is used to read the current 1PPS PID proportional coeff (Kp). Where first 4 byte are zero, and 4 last byte is a message.	

COMMAND ID	COMMAND NAME	TYPE	INPUT	RESPONSE	REMARKS	EXAMPLE
85	1PPS PID Differential Coeff	Set	?DEV:85:0000XXXX <CR/LF>	?DEV:OK<CR/LF>	This command is used to set the current 1PPS PID differential coeff (Kd). XXXX – 4 bytes with signed data. Most significant bit is the sign.	?DEV:85:1FFF – positive number, ?DEV:85:FFFF – negative number
		Request	?DEV:85?<CR/LF>	?DEV:85:0000XXXX<CR/LF>	This command is used to read the current 1PPS PID differential coeff (Kd). Where first 4 byte are zero, and 4 last byte is a message.	
86	1PPS frequency correction word	Request	?DEV:86?<CR/LF>	?DEV:85:XXXXXXXX<CR/LF>	This command is used to read the current frequency offset referred to 1 PPS tracking. 1 bit corresponds to 1.597E-14 parts of the output frequency	?DEV:85:000003FF means that at the moment 1PPS tracking algorithm sets frequency offset 1023x1.597E-14= ~1.663E-11
		Set	?DEV:86:00000001	?DEV:OK<CR/LF>	This command is used to set the current frequency offset referred to 1 PPS tracking to zero. This command updates only RAM value. Use command #18 if required.	
87	1PPS Gate	Request	?DEV:87?<CR/LF>	?DEV:87:XXXXXXXX<CR/LF>	This command is used to read the current phase difference between internal 1PPS and incoming pulse in terms of 2.16 ns	1 bit corresponds to 2.16 ns difference (gate). ?DEV:87:00000003 means that 3x2.16ns = 6.48 ns difference exists between the last incoming pulse and internal 1 PPS signal
88	Multifunctional output pin mode	Set	?DEV:88:0000000X <CR/LF>	?DEV:OK<CR/LF>	This command is used to set output pin mode (stored in FLASH): 1: 1PPS out; 2: Inverted 1PPS out; 3: High level; 4: Low level; 5: Selected Status bit (Use command #19); 6: Inverted Selected Status bit (Use command #19).	
		Request	?DEV:88?<CR/LF>	?DEV:88:0000000X<CR/LF>	This command is used to read the current Internal 1PPS status. . Where first 7 byte are zero, and 1 last byte is a status(1 – enabled, 0 – disabled).	